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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,718	05/03/2001	Gert Burbach	2000.064400/DE0058	8412

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EXAMINER	
BERRY, RENEE R	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/848,718	Burbach et al.
Examiner	**Art Unit**
Renee Berry	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-15 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent no. 6,174,794 to Gardner et al. in view of US patent no. 6,429,477 to Mandelman et al.

Gardner teaches a method of forming a substrate contact in a field effect transistor by providing a substrate with an insulation layer formed thereon; forming a semiconductor layer above the insulation layer; forming a transistor in an active region of the semiconductor layer; forming a first part of the substrate contact, first part extending through the insulation layer and contacting the substrate, the first part having a first end that extends above a surface of the semiconductor layer; and contact, and the second part being electrically coupled to the first end of the first part of the substrate contact at column 10, lines 57-67 to column 11, lines 1-8, claim 1.

In regard to claim 2, Gardner teaches depositing a dielectric layer stack having a stop layer in contact with a gate electrode of the field effect transistor; thinning and planarizing the dielectric layer stack, wherein material of the dielectric layer stack is maintained over the gate electrode with a predefined thickness that insures coverage of the gate electrode; forming a first substrate

opening in the dielectric layer stack, the semiconductor layer and the insulation layer by photolithography and etching; filling the first substrate opening with a contact metal to form the first part; removing excess contact metal from the dielectric layer stack to planarize the surface of the dielectric stack; depositing a dielectric layer with a predefined thickness over the dielectric layer stack and the first substrate opening and a gate contact at column 10, lines 57-67 to column 11, lines 1-8, claim 1.

In regard to claim 5, Gardner teaches the dielectric layer stack is deposited by plasma enhanced chemical vapor deposition at column 6, lines 3-5.

In regard to claim 7, Gardner teaches removing the excess contact metal by chemically mechanically polishing the surface so as to avoid any cavities formed therein at column 9, lines 19-21 and 29-31.

In regard to claim 10, Gardner teaches the contact metal and the second contact metal are the same at column 5, lines 38-46.

In regard to claim 12, Gardner teaches the constant is less than 40 at column 5, lines 59-65.

In regard to claim 13, Gardner teaches the stop layer serves as an anti-reflecting coating (silicon nitride) at column 6, lines 60-65.

In regard to claim 14, Gardner teaches the stop layer having one silicon nitride and silicon oxynitride at column 6, lines 60-65.

In regard to claim 15, Gardner teaches the material of the dielectric layer stack that is maintained over the gate electrode having material of the stop layer at column 6, lines 60-65.

However, Gardner does not teach all the limitations of the claims.

In regard to claim 2, Mandelman teaches forming a second substrate contact opening over and aligned to the first part; forming in the dielectric layer stack and the dielectric layer, by using the stop layer, a drain contact opening over the drain region, a source contact opening over the source region, and a gate contact opening over the gate electrode; filling the second substrate contact opening with a second contact metal, thereby forming a second part; and filling the drain contact opening, the source contact opening, and the gate contact opening with the second contact metal, thereby forming a drain contact, a source contact at column 10, lines 31-43, claim 1b-e

In regard to claim 3, Mandelman teaches forming the second substrate contact opening, the drain contact opening, the source contact opening, and the gate contact opening is performed during the same etch process at column 10, lines 53-55, claim 5.

In regard to claim 4, Mandelman teaches filling the second substage contact opening and filling the drain contact opening, the source contact opening, and the gate contact opening is performed during the same filling process at column 9, lines 47-55.

In regard to claim 6, Mandelman teaches the first substrate contact opening is formed so as to extend into the substrate at column 10, lines 30-37, claim 1b and 1c .

In regard to claim 8, Mandelman teaches forming the second substrate contact opening, the drain contact opening, the source contact opening, and the gate contact opening is performed by simultaneously etching while the contact metal provides a high selectivity in removing material of the dielectric layer at column 5, lines 57-65 and column 6, lines 40-49.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Gardner to include forming a second substrate contact opening over and aligned to the first part; forming in the dielectric layer stack and the dielectric layer, by using the stop layer, a drain contact opening over the drain region, a source contact opening over the source region, and a gate contact opening over the gate electrode; filling the second substrate contact opening with a second contact metal, thereby forming a second part; and filling the drain contact opening, the source contact opening, and the gate contact opening with the second contact metal, thereby forming a drain contact, a source contact; filling the second substage contact opening and filling the drain contact opening, the source contact opening, and the gate contact opening is performed during the same filling process; the first substrate contact opening is formed so as to extend into the substrate; forming the second substrate contact opening, the drain contact opening, the source contact opening, and the gate contact opening is performed by simultaneously etching while the contact metal provides a high selectivity in removing material of the dielectric layer, since such a modification would result in improved performance as described in column 2, lines 30-35 of Mandelman et al.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. R. Berry whose telephone number is (703) 305-4544.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

RRB

April 21, 2003